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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/731,566	12/08/2003	Gilbert C. Vandling	6450.P003	5068

8791 7590 08/25/2006

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EXAMINER	
SIEK, VUTHE	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 08/25/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/731,566	VANDLING, GILBERT C.	
	Examiner	Art Unit	
	Vuthe Siek	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 June 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8,10-16,21-24 and 26-31* is/are rejected.

7)☒ Claim(s) *9,17-20,25 and 32-35* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 June 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *6/15/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to application 10/731,566 and amendment filed on 6/15/2006. Claims 1-35 remain pending in the application.

Claim Objections

2. Claim 4, 11, 16, 24 and 31 are objected to because of the following informalities: claims 4, 11 and 24, "the design" should be changed to --the sequential logic design--, to properly define the claim language; claim 16, "selected from a group comprising" should be changed to –selected from a group consisting of--, to properly correct Markus claim format; claim 31, "(Previously Presented)" should be changed to --(Currently Amended)--, to properly define the status of the claim. Appropriate correction is required.

3. The indicated allowability of claims 15 and 31 are withdrawn in view of the newly discovered reference(s) to Girard et al., "A Trace-Based Method for Delay Fault Diagnosis in Synchronous Sequential Circuits," IEEE, 1995, pages 526-532. Rejections based on the newly cited reference(s) follow.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-8, 10-16, 21-24 and 26-31 are rejected under 35 U.S.C. 102(b) as being anticipated by Girard et al., "A Trace-Based Method for Delay Fault Diagnosis in Synchronous Sequential Circuits," IEEE, 1995, pages 526-532.

6. As to claims 1, 5 and 21, Girard et al. teach a trace-based method for delay fault diagnosis in synchronous sequential circuits (see pages 526-532). The method comprises forming modeling for sequential circuits, where a sequential circuit can be modeled as composed of a combinational part and a memory part. Fig. 1 show iterative array model for a sequential circuit that is formed by an array of combinational circuits. The method also comprises simulating each stage of clocking sequence (slow clock and fast clock) on the sequential logic design as described above to produce simulation values and saving the simulation values (page 528, under section 5, Girard et al. teach the signal values on each line in the activation and propagation phases are recorded in order to be used later by the critical path tracing process. Again, Girard et al. teach starting page 528 under section 5. The trace-based method to provide an equivalent combinational logic representation of the sequential logic design.

7. As to claims 15 and 31, remarks set forth in rejecting claims 1, 5 and 21 equally apply. In addition, Girard et al. teach performing trace-based process based on time frame corresponding to time frame i-1 (a time T being negative) and time frame i+1 (a time T being not negative) (see section 5.1, page 529). The multi-valued simulations on these time frames comprise unknown logic (value X) and a known simulation value (0, 1 values) as described on page 529.

8. As to claims 2 and 22, Girard et al. teach for each time "T" (time frame) of the clocking sequence, each block being measured at the time T is traced (see Fig. 1-4, see section 5. The trace-based method).

9. As to claims 3 and 23, Girard et al. teach circuit modeling for sequential circuits that is composed as of a combinational pare and a memory part. The boundaries of the combinational logic consist of primary inputs (data input), primary outputs (data output) and flip-flops (FF's) (Fig. 1). Section 5 describes a trace-based method for sequential circuits including a multi-values simulations and critical path tracing, where a primary output is traced backed (see section 5.1-5.2).

10. As to claims 4 and 24, Girard et al. teach multi-valued simulations for sequential circuits (starting page 529). Since the sequential circuits includes flip-flops or memory part (scan cells), simulating the sequential circuits as taught by Girard et al. include simulating scan operations by placing the sequential circuit in its scan state (see section 3, page 528).

11. As to claim 6, Girard et al. teach at the end of initialization sequence, all flip-flops (scan cells) are set into states required by the fault activation vector. Next, the fault is activated by applying Vi and using a fast clock. Concepts of testing for delay faults in combinational or scan-based circuits are applicable in this phase (see section 3, page 528). The scan-based circuits testing require setting scan control inputs to their scan-enable values.

12. As to claims 7-8, Girard et al. teach simulating sequential circuits by modeling the circuit as combinational circuit part and memory part to provide equivalent

combinational circuit (Fig. 1). The simulation is performed by slow clock and fast clock, therefore in order to perform with fast clock, the rest of clocks (slow clock) must be turned off.

13. As to claim 10, Girard et al. teach a method for diagnosing gate delay faults in synchronous sequential circuits based on a path tracing algorithm appropriate sequential circuits to produce a combinational circuit equivalent (see section 6).

14. As to claims 11-12 and 27-28, Girard et al. teach modeling sequential circuits as a combination part and memory part (partitioning the sequential design into smaller pieces) and processed on separate computing device (see section 2).

15. As to claims 13 and 29, Girard et al. simulating the sequential circuits based on fast clock cycles (sampled clock or chopped clocks) (see section 4).

16. As to claims 14 and 30, Girard et al. simulating the sequential circuits based on fast clock cycles (chopped clocks) and the signal values on each line in activation and propagation phases are recorded in order to be used later by the critical path tracing process (see page 528, section 5).

17. As to claim 16, Girard et al. teach the known simulation value is 0 or 1 (page 528 section 5).

18. As to claim 26, Girard et al. teach the operations are used for automatic test pattern generation (See section 4).

Allowable Subject Matter

19. Claims 9, 17-20, 25 and 32-35 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The prior art of record does not teach or fairly suggest the claim limitations are recited in claims 17 and 19-20.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vuthe Siek whose telephone number is (571) 272-1906.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on (571) 272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Vuthe Siek

VUTHE SIEK
PRIMARY EXAMINER